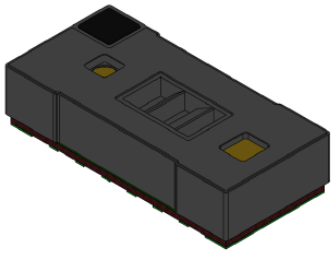
VL53L5

Datasheet

Time-of-Flight mini depth camera



Features

- Fully integrated miniature module
  - Emitter: 940 nm invisible vertical cavity surface emitting laser (VCSEL) and integrated analog driver
  - 61 ° diagonal square system field of view (FoV) using diffractive optical elements (DOE) on both transmitter and receiver
  - Receiving array of single photon avalanche diodes (SPADs)
  - Low-power microcontroller running Firmware
  - Size: 6.4 x 3.0 x 1.5 mm
- Fast, accurate distance ranging
  - Parallel multi zone output; either 4x4 or 8x8 separate regions of interest (ROI)
  - Up to 400 cm ranging
  - 60 Hz frame rate capability
  - Histogram processing and algorithmic compensation minimizes or removes impact of cover glass crosstalk
  - Dynamic crosstalk compensation for fingerprint smudge via latest patented ToF techniques
- Easy integration
  - Single reflowable component
  - Flexible power supply options, single 3.3 V or 2.8 V operation or combination of either 3.3 V or 2.8 V AVDD with 1.8 V IOVDD
  - Compatible with wide range of cover glass materials
  - I²C or SPI interface
  - Low-power pin and two general purpose inputs (GPIOs) for interrupt and synchronization
  - Full set of software drivers (Linux and Android compatible) for turnkey ranging

Applications

- Laser assisted autofocus (LAF). Enhances the camera AF system speed and robustness especially in difficult low light or low contrast scenes. Ideal companion for phase detection autofocus (PDAF) sensors.
- Scene understanding. Multi-zone and multi-object distance detection enables touch-to-focus or focus bracketing for best shot selection.
- Camera assist. Further camera assistance by enabling flash dimming, indoor/outdoor detection and background removal assist
- Augmented reality/virtual reality (AR/VR) enhancement. Dual camera stereoscopy and 3D depth assistance thanks to multi zone distance measurement
- Video focus tracking. 60 Hz ranging allows optimization of continuous focus algorithm
- Enhances camera bokeh performance through captured scene depth data

Description

The VL53L5 is a state of the art, Time-of-Flight (ToF), laser-ranging sensor enhancing the ST FlightSense product family. Housed in a miniature reflowable package, it integrates a SPAD array, physical infrared filters, and diffractive optics (DOE) to achieve the best ranging performance in various ambient lighting conditions with a range of cover glass materials.

The use of a DOE above the vertical cavity surface emitting laser (VCSEL) allows a square FoV to be projected onto the scene. The reflection of this light is focused by the receiver lens onto a SPAD array.

Unlike conventional IR sensors, the VL53L5 uses ST's latest generation, direct ToF technology which allows absolute distance measurement whatever the target color and reflectance. It provides accurate ranging up to 400 cm and can work at fast speeds (60 Hz), which makes it the fastest, multi-point, miniature ToF sensor on the market.

With patented algorithms and ingenious module construction, the VL53L5 is also able to detect different objects within the FoV with depth information at 60 Hz.

Scene browsing and multi zone detection is possible with the VL53L5 thanks to a software customizable detection array to achieve a quicker touch-to-focus or mini depth map.

1 Product overview

1.1 Technical specifications

Table 1. Technical specifications

Feature	Details
Package	Optical LGA16
Size	6.4 x 3.0 x 1.5 mm
Ranging	0 to 400 cm per zone
Operating voltage	IOVDD: 1.8 or 2.8 V or 3.3 V AVDD: 2.8 V or 3.3 V
Operating temperature	-30 to 85 °C
Sample rate	Up to 60 Hz
Infrared emitter	940 nm
I^2C and SPI interfaces	I^2C: 1 MHz serial bus, address: 0x52 SPI: 20 MHz

1.2 Field of view

The Field of view (FoV) of the module may be defined as an angle between the horizontal and vertical edges, and is with reference to the RX aperture.

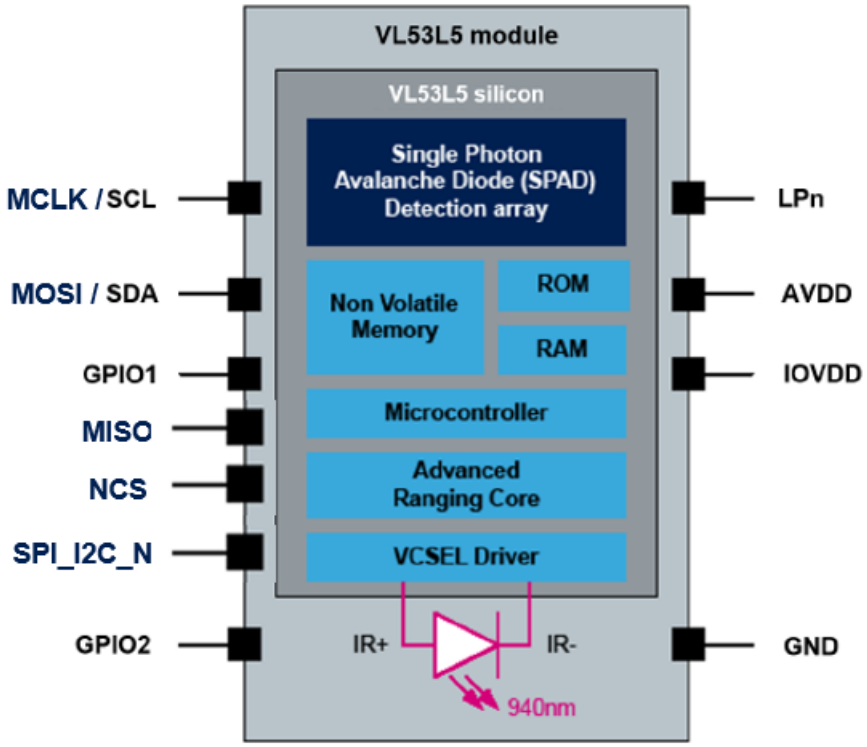
Table 2. FoV angles

	Horizontal	Vertical
Half angle (centre to edge)	21.75°	21.75°
Full angle (edge to edge)	43.5°	43.5°

Note: The system FoV is smaller than the exclusion cones referenced in the outline drawings in section 7 which should be used as reference for coverglass design.

1.3 System block diagram

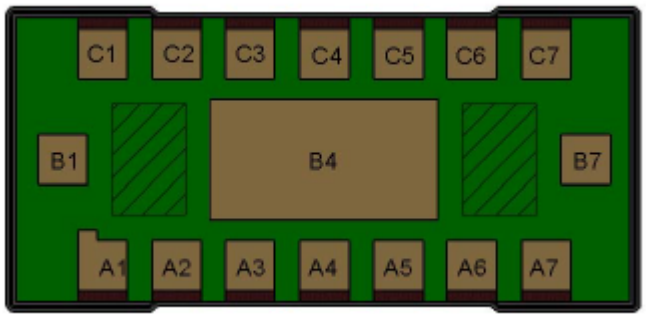
Figure 1. **VL53L5 block diagram**



1.4 Device pinout

The figure below shows the pinout of the VL53L5.

Figure 2. **VL53L5 pinout (bottom view)**



The VL53L5 pin description related to the I^2C and SPI configuration is given in the table below. For those pins that support both I^2C and SPI protocol, the I^2C description is listed first and the SPI second.

Table 3. **VL53L5 pin description - I^2C and SPI configuration**

Pin number	Signal name	Signal type	Signal description
A1	SPI_I2C_N	Digital input	**I^2C:** connect to ground

Pin number	Signal name	Signal type	Signal description
		Digital input	**SPI:** connect to IOVDD
A2	NCS		**I²C:** connect to ground **SPI:** active low chip select
A3	GPIO1	Digital input/output (I/O)	Interrupt output, defaults to open-drain output (tri-state), pull-up resistor to IOVDD required
A4	IOVDD	Power	1.8 V, 2.8 V or 3.3 V supply for digital core and I/O supply
A5	LPn	Digital input	Comms enable. Drive this pin to logic 0 to disable the I²C comms when the device is in LP mode. Drive this pin to logic 1 to enable I²C comms in LP mode. Typically used when it is required to change the I²C adress in multi-device systems. Connect to IOVDD if not used or interfacing via SPI
A6	Not used	Test	Connect to ground
A7			
B1	AVDD	Power	2.8 V or 3.3 V analog and VCSEL supply
B4	THERMAL PAD	Ground	Connect to a ground plane to allow good thermal conduction
B7	AVDD	Power	2.8 V or 3.3 V analog and VCSEL supply
C1	GND	Ground	Ground
C2	GPIO2	Digital I/O	General purpose I/O, defaults to open-drain output (tri-state), pull-up resistor to IOVDD required
C3	SDA / MOSI		**I²C:** data (bidirectional), pull-up resistor required to IOVDD **SPI:** master output slave input
C4	SCL / MCLK	Digital input	**I²C:** clock (input), pull-up resistor required to IOVDD **SPI:** master clock
C5	MISO	Digital output	**I²C:** do not connect **SPI:** master input slave output. push-pull driven to IOVDD level
C6	Not used	Test	Connect to ground
C7	GND	Ground	Ground

Note: The thermal pad pin has to be connected to ground (see AN5228 "VL53L5 thermal guidelines Time-of-Flight ranging sensor with multi-object detection).

Note: All digital signals must be driven to the IOVDD level.

1.5 Application schematic

The figures below show the application schematic of the VL53L5 in I²C protocol configuration.

Figure 3. 1.8 V host configuration - I²C setup

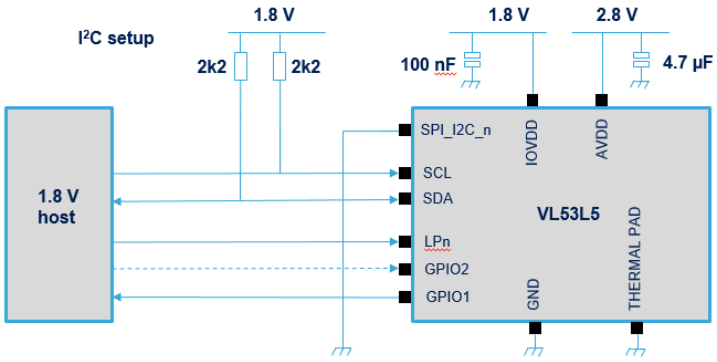


Figure 4. 2.8 V host configuration - I²C setup

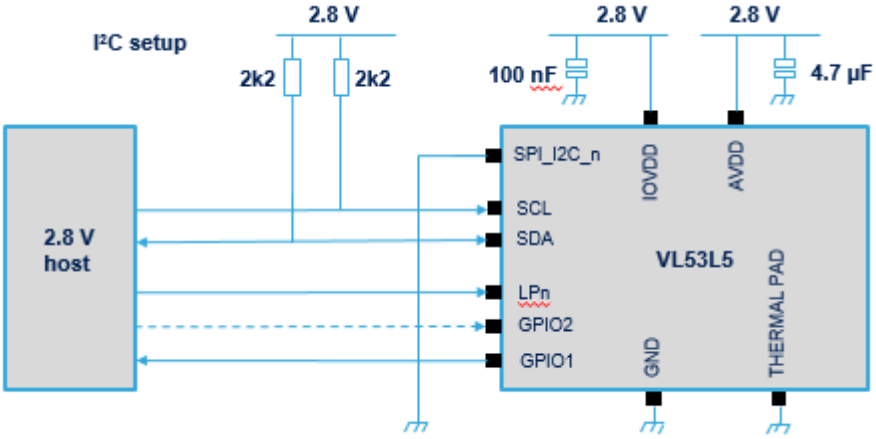
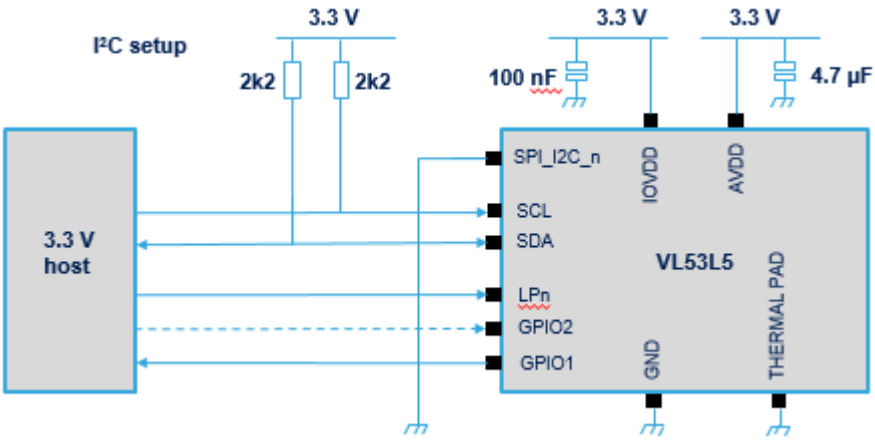


Figure 5. 3.3 V host configuration - I²C setup



Note: Capacitors on the external supplies (AVDD and IOVDD) should be placed as close as possible to the module pins.

The figures below show the application schematic of the VL53L5 in SPI protocol configuration.

Figure 6. 1.8 V host configuration - SPI setup

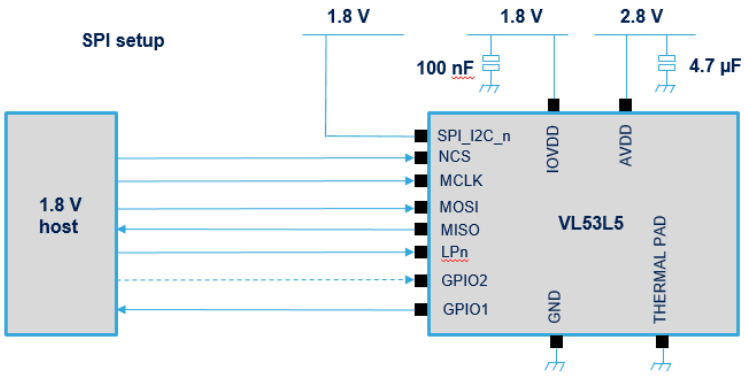


Figure 7. 2.8 V host configuration - SPI setup

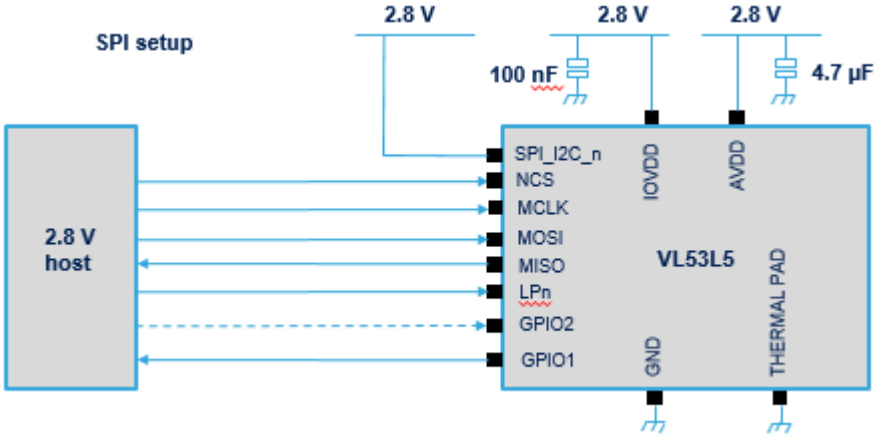
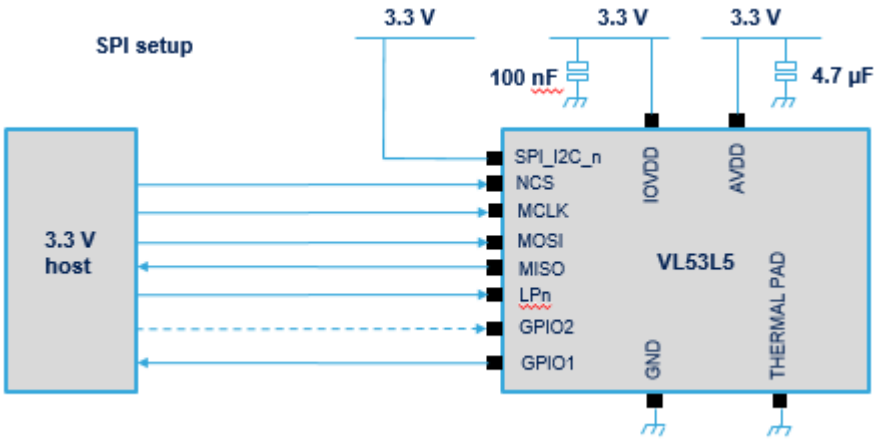


Figure 8. 3.3 V host configuration - SPI setup



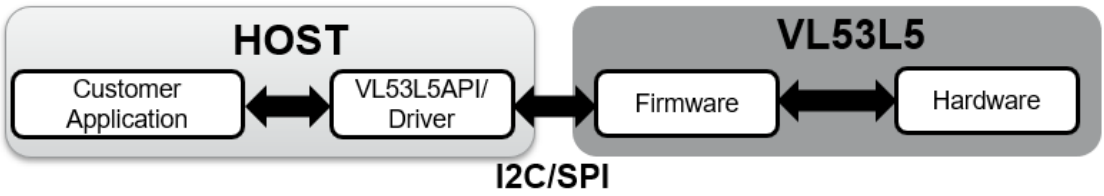
Note: Capacitors on the external supplies (AVDD and IOVDD) should be placed as close as possible to the module pins.

2 Functional description

2.1 Software interface

This section shows the software interface of the device. The host customer application controls the VL53L5 using an application programming interface (API). The API implementation is delivered to the customer as a driver (bare C code and reference Linux/Android driver). The bare driver provides the customer application with a set of high level functions that allow control of the VL53L5 Firmware such as device initialization, ranging start/stop, mode select etc.

Figure 9. VL53L5 system functional description



2.2 Power state machine

Figure 10. **Power state machine**

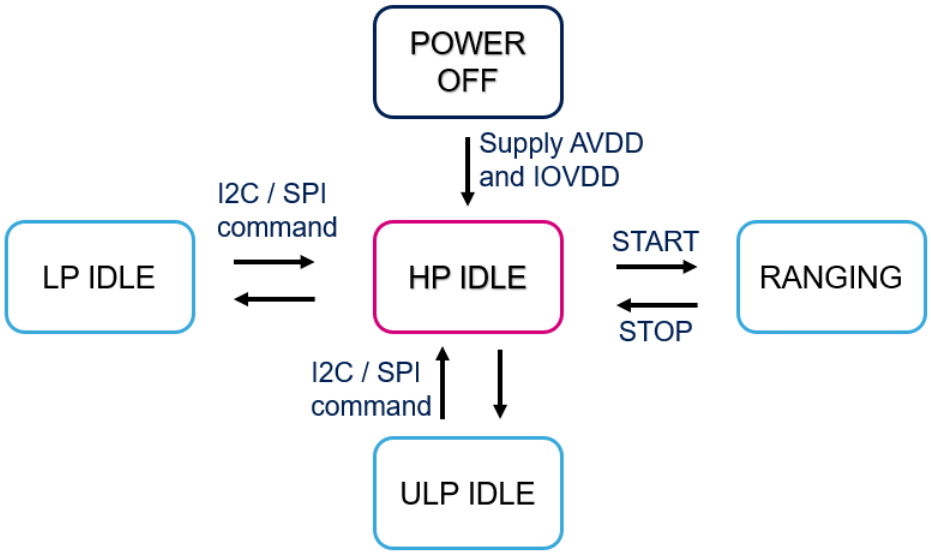


Table 4. **Power state description**

Device state	Description
ULP idle	Lowest power state (LP and HP regulators disabled) All data in RAMs and register are lost Re-initialization required
LP idle	Low power idle state with data retention (LP regulator enabled) RAM and register content retained Allows fast resume to HP idle I^2C communication disabled if using LPn
HP idle	High power idle state (LP and HP regulator enabled) Device needs to be in HP idle state to start ranging Power up state
Ranging	Full operation VCSEL is active (pulsing)

2.3 Power up sequence

The recommended power up sequence is shown in the figure below. When powering up the device, the IOVDD supply should be applied at the same time or after AVDD. When removing power, the AVDD supply should be removed at the same time or after IOVDD.

Note: avoid powering IOVDD while AVDD is unpowered to prevent increased leakage current.

Figure 11. Power up sequence

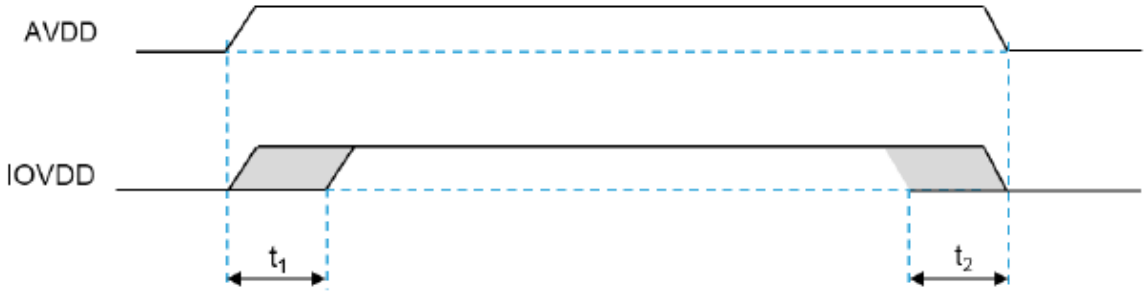


Table 5. Power up timing table

Time	Description	Min.
t_1	IOVDD rise after AVDD	0 s
t_2	IOVDD fall before AVDD	0 s

2.3.1 Power up slew

To ensure proper operation of the module, the following minimum slew rates on the supplies must be met for correct operation of the power on reset (POR) circuitry. The POR circuitry triggers at 0.9 V, but the supplies should reach their operation levels in accordance with the slew rates listed in the table below.

Figure 12. Power up slew

Note: The minimum reset time is the minimum time required for the device ROM to load and boot up after IOVDD reaches the POR rising threshold. The supply must have reached the minimum operating level (1.6V) within this time.

Note: The minimum slew rate on the IOVDD is the same regardless of 1.8 V or 2.8 V operation.

Note: The AVDD rise time is determined by the internal analogue levels which must be stable for correct operation.

Table 6. Supply slew rate minimum limits

Supply status	AVDD slew	IOVDD slew
Start together	0.001 V/µs	0.012 V/µs
AVDD stable followed by IOVDD	—	0.012 V/µs
IOVDD stable followed by AVDD	0.001 V/µs	—

2.3.2 Power up and I^2C access

For correct operation of the device, the I^2C interface assumes the power level has reached 1.62 V.

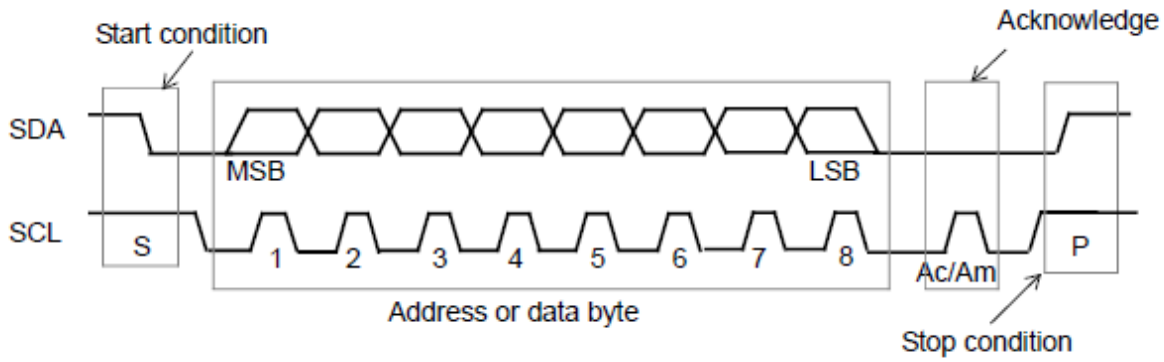
3 I²C control interface

This section specifies the control interface. The I²C interface uses two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus uses a unique address and a simple master / slave relationships exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high.

Clock signal (SCL) generation is performed by the master device. The master device initiates data transfer. The I²C bus on the VL53L5 has a maximum speed of 1 Mbits/s and uses a device 8-bit address of 0x52.

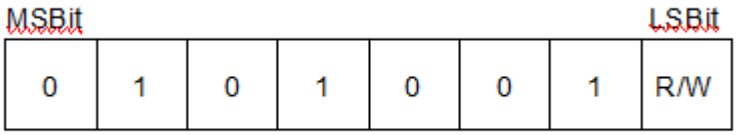
Figure 13. Data transfer protocol



Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for VL53L5 acknowledge and Am for master acknowledge (host bus master). The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

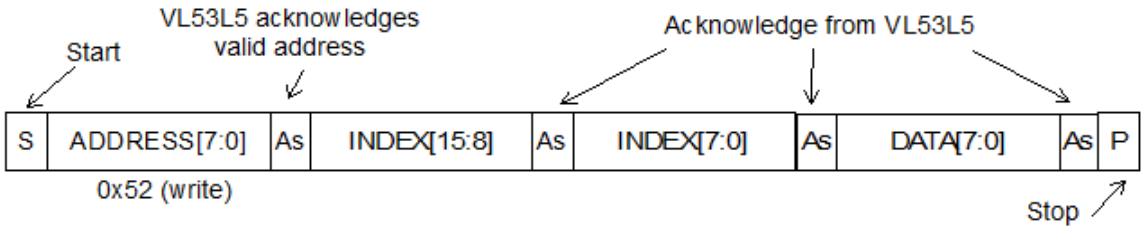
A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x52) and also specifies the data direction. If the least significant bit is low (that is, 0x52) the message is a master-write-to-the-slave. If the lsb is set (that is, 0x53) then the message is a master-read-from-the-slave.

Figure 14. VL53L5 I²C device address: 0x52



All serial interface communications with the camera module must begin with a start condition. The VL53L5 module acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (lsb of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence, the second byte received provides a 16-bit index which points to one of the internal 8-bit registers.

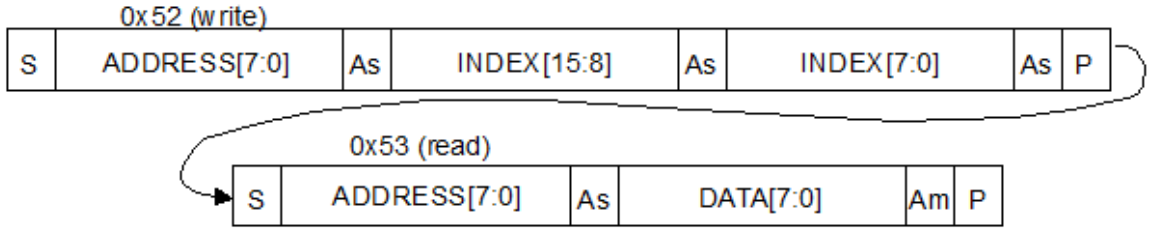
Figure 15. **VL53L5 data format (write)**



As data are received by the slave, they are written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data are then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 16. **VL53L5 data format (read)**



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the VL53L5 for a write and the host for a read).

A message can only be terminated by the bus master, either by issuing a stop condition or by a negative acknowledge (that is, not pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a stop condition. If the auto-increment feature is used the master does **not** have to send address indexes to accompany the data bytes.

Figure 17. **VL53L5 data format (sequential write)**

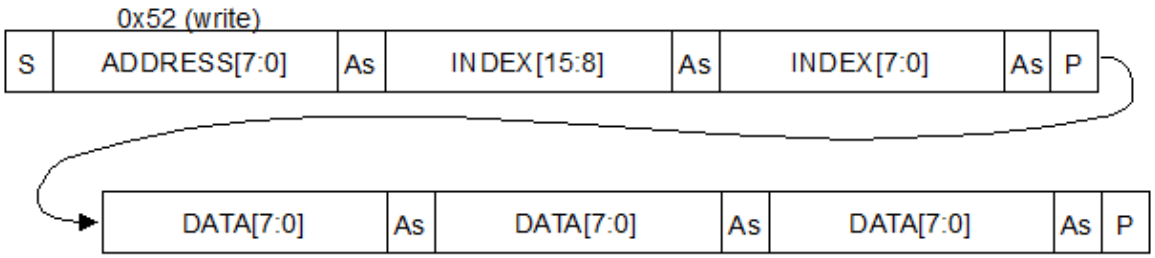
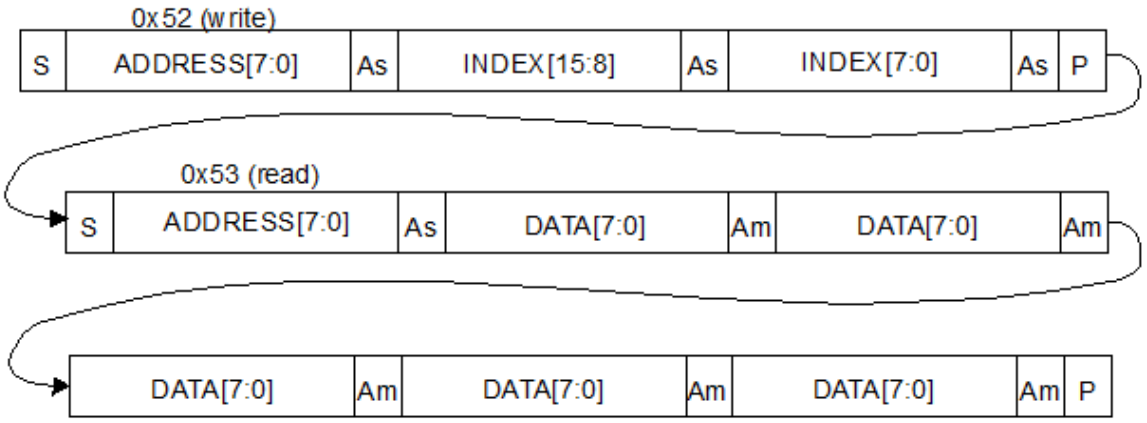


Figure 18. **VL53L5 data format (sequential read)**



3.1 I²C interface - timing characteristics

Timing characteristics are shown in the tables below. Please refer to the figure below for an explanation of the parameters used.

Timings are given for all PVT conditions.

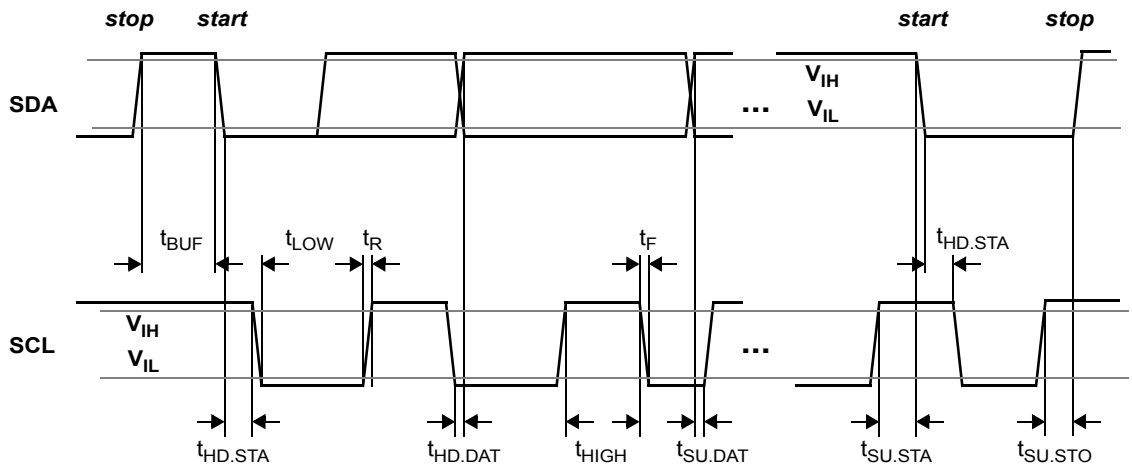
Table 7. I²C interface - timing characteristics for Fast mode plus (1 MHz)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	1000	kHz
t_{LOW}	Clock pulse width low	0.5	—	—	µs
t_{HIGH}	Clock pulse width high	0.26	—	—	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	0.5	—	—	ms
$t_{HD.STA}$	Start hold time	0.26	—	—	µs
$t_{SU.STA}$	Start setup time	0.26	—	—	µs
$t_{HD.DAT}$	Data in hold time	0	—	0.9	µs
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	120	ns
t_F	SCL/SDA fall time	—	—	120	ns
$t_{SU.STO}$	Stop setup time	0.26	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	pF
C_L	Load capacitance	—	140	550	pF

Table 8. I²C interface - timing characteristics for Fast mode (400 kHz)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	400	kHz
t_{LOW}	Clock pulse width low	1.3	—	—	µs
t_{HIGH}	Clock pulse width high	0.6	—	—	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	1.3	—	—	ms
$t_{HD.STA}$	Start hold time	0.26	—	—	µs
$t_{SU.STA}$	Start setup time	0.26	—	—	µs
$t_{HD.DAT}$	Data in hold time	0	—	0.9	µs
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	120	ns
t_F	SCL/SDA fall time	—	—	120	ns
$t_{SU.STO}$	Stop setup time	0.6	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	pF
C_L	Load capacitance	—	125	400	pF

Figure 19. I²C timing characteristics



4 SPI timing specification

This section specifies the SPI control interface used for control data transfer.

The communication interface is based on a 4-wire serial synchronous interface between the host (master) and the VL53L5 (slave device) see schematics in Section 1.4. The 4-wire interface comprises the following four signals:

- NCS: chip select (active low)
- MCLK: master serial clock
- MOSI: master output slave input, data output from master
- MISO: master input slave output, data output from slave

All signals are CMOS inputs/outputs, with levels in line with the IOVDD supply.

The SPI modes supported are clock polarity = 1 and clock phase = 1, which corresponds to data captured on a clock's rising edge and data propagated on a falling one. The master selects the slave device with NCS. NCS is the slave transmit enable and it is an active low signal. After the device is selected with the falling edge of NCS, an 8-bit command can be received. If VL53L5 has not been activated using the NCS chip select line, the MCLK input clock and MOSI signals are disregarded.

The falling edge (high to low transition) of the NCS signal is required to initiate an action. The transmission ends with the rising edge (low to high transition) that causes the end of data transfer, resets the internal counter and command registers. While the register address is applied on the MOSI pin, the same information is being mirrored on the MISO pin.

This reinitializes the serial communication. NCS can be reset to a non-communication state (high) at any time including during a transaction. Should this happen, the device resets its internal state machine, any on-going communications are aborted without internal changes to the registers taking place, so that the interface is ready to receive a new transaction again. However the SPI slave can tolerate the MCLK being interrupted and can resume at any point in time, without specific duration limit.

During each SPI clock cycle, a full duplex data transmission occurs. MOSI input is the data signal, provided by the host to the device. It carries both address and data information in Write mode, and only address information in Read mode. The master sends a bit on the MOSI line and the slave reads it, while the slave sends a bit on the MISO line and the master reads it. This sequence is maintained even when only one-directional data transfer is intended.

MISO output is the data signal, provided by the device to the host. It carries the data in Read mode only as well as the mode register content during the address setup. Any internal register that can be written to, can also be read from. There are also read-only registers that contain device status information, for example, design revision details. A read instruction from an unused register location returns the value 0x00. A read instruction from the manufacturer's specific registers may return any value. A write instruction to a reserved or unused register location is illegal and the effect of such a write is ignored. Transmission may continue for any number of clock cycles. When complete, the master stops toggling the clock signal, and typically deselects the slave.

Table 9. SPI interface timing specification

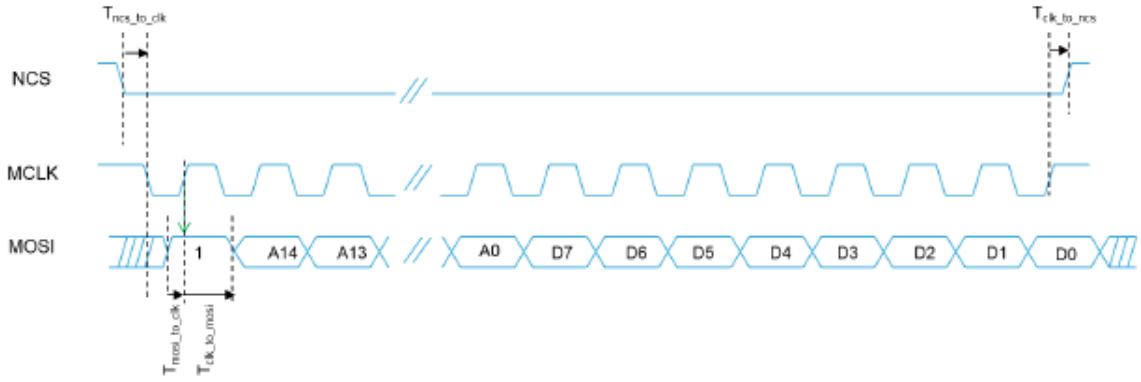
Parameter	Symbol	Min.	Max.	Unit	Notes
Operating frequency	F_{spi}	—	20	MHz	MCLK
Time from NCS active and MCLK falling edge	$T_{ncs\_to\_clk}$	0	—	ns	
Rise/Fall time on MISO	$T_{riseFallMiso}$	—	3	ns	With 20 pF load max
Duty cycle	Duty	40	60	%	
Time from MOSI stable to MCLK rising edge	$T_{mosi\_to\_clk}$	16	—	ns	
Time MOSI must remain stable after MCLK rising edge	$T_{clk\_to\_mosi}$	16	—	ns	
Time from last MCLK rising edge to NCS going inactive	$T_{clk\_to\_ncs}$	0	—	ns	
Propagation delay from falling MCLK edge to MISO data valid	$T_{clk\_to\_dat}$	—	18	ns	With 20 pF load max
Min. MCLK high time going into Read mode	T_{clk_read}	267	—	ns	

4.1 SPI write messages

The write timing sequence is showed in the figure below. Once NCS selects the device, the master sends a write command to the VL53L5. The master then provides a clock to output the status. The writing sequence starts with the MOSI initial value equal to 1, the address is sent first and data afterwards. The most significant bit is sent first (big-endian format). The address length is 15 bits. Data length is 8 bits.

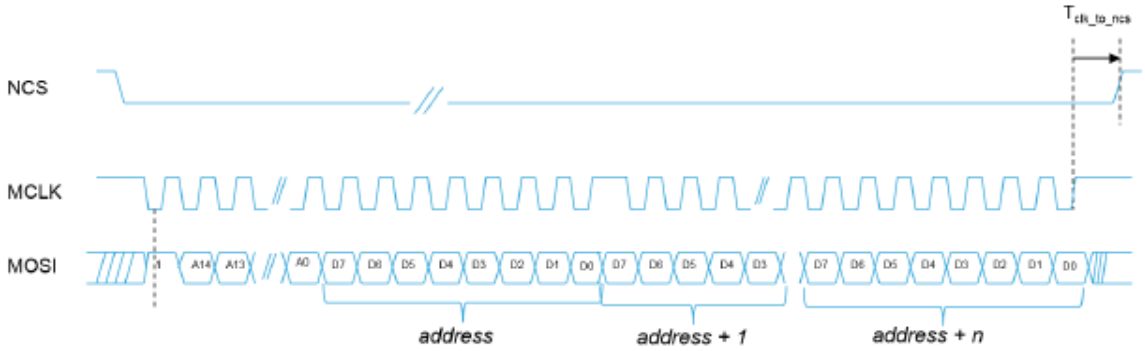
See Table 9. SPI interface timing specification for the SPI timing values.

Figure 20. SPI writing timing sequence



If the host continues to transmit data beyond the first 8 data bits, then the slave goes into Auto-increment write mode. The Auto-increment write timing sequence is shown in the figure below.The MOSI initial value is 1. The address is incremented automatically and internally by the slave. Subsequent data bits correspond to incrementing addresses.

Figure 21. **SPI auto-increment write sequence**

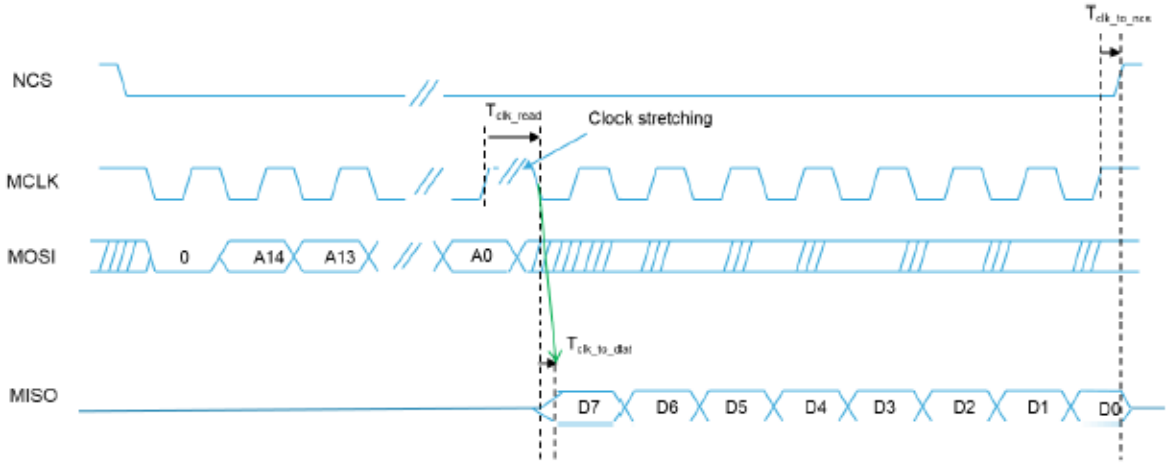


4.2 SPI read messages

The master sends the read command to VL53L5. The master then provides a clock to output the status.

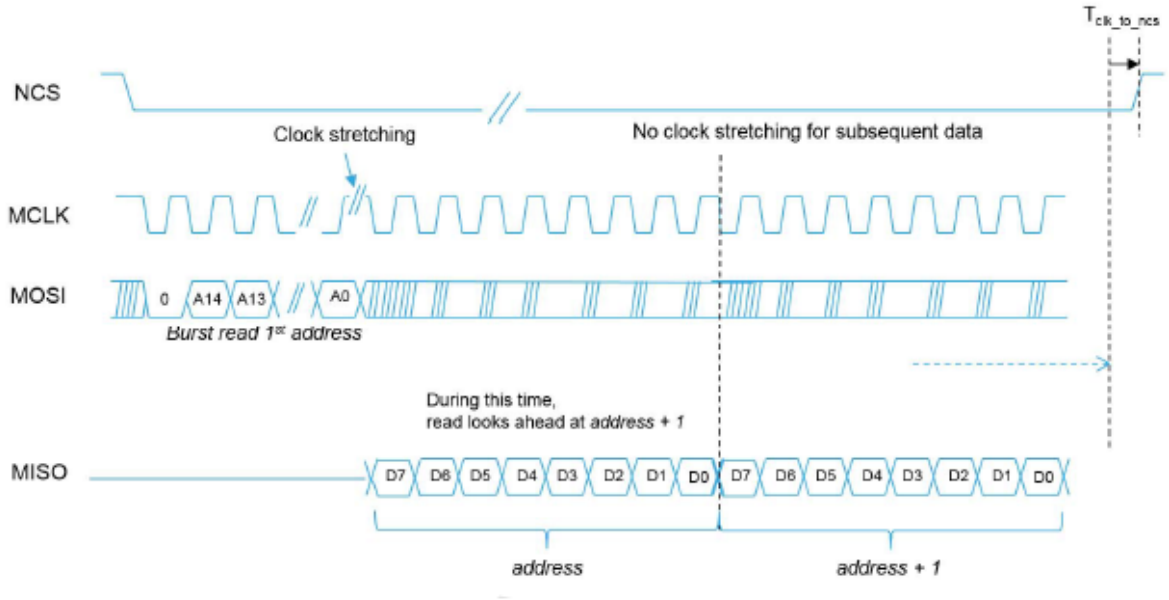
In Read mode, the slave reads the data and then transmission is ended by the master. The reading sequence starts with the first value of the MOSI equal to 0. The most significant bit is sent first (big-endian format). Once the last bit of the address has been received, the host holds the MCLK high for time equal to Tclk_read. This stretching of the clock allows enough time for the read data to reach the slave from the register bank being accessed. After that, the host resumes toggling the MCLK and the read data appear on the MISO line, with the most significant bit first (big-endian format). Once 8 bits of data have been received, the host sets NCS high terminating the process. More details for the SPI read timing are shown in the figure below.

Figure 22. **SPI read timing (with clock stretching)**



If the host continues to toggle the MCLK after the last data bit has been read, the slave goes into Auto-increment read mode. In this mode, the address is automatically incremented by the slave and the read data are transmitted sequentially to the master on the MISO line. In this mode, no further clock stretching is required beyond the one after the initial address transmission. More details for the SPI auto-increment Read mode are shown in the figure below.

Figure 23. **SPI auto-increment read sequence**



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 10. Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
AVDD, IOVDD	-0.5	—	3.6	V
SCL, SDA, LPn, GPIO1 and GPIO2	-0.5	—	3.6	

Note: Stresses above those listed in Section 1 Product overview may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended operating conditions

Table 11. Recommended operating conditions

Parameter		Min.	Typ.	Max.	Unit
AVDD supply(1)	2.8 V configuration	2.5	2.8	3.3	V
	3.3 V configuration	3.0	3.3	3.6	
IOVDD supply	1.8 V configuration	1.62	1.8	1.98	
	2.8 V configuration	2.5	2.8	3.3	
	3.3 V configuration	3.0	3.3	3.6	
Ambient temperature (normal operating)		-30	—	85	°C

1. *AVDD is independent of IOVDD*

5.3 Electrostatic discharge (ESD)

The VL53L5 is compliant with ESD values presented in the table below.

Table 12. ESD performances

Parameter	Specification	Conditions
Human body model	JEDEC JS-001-2014	± 2 kV, 1500 Ohms, 100 pF
Charged device model	JEDEC JS-002-2014	± 500 V

5.4 Current consumption

The current consumption values are given in the table below.

- Typical values quoted are for nominal voltage, process, and temperature (23°C).
- Maximum values are quoted for worst case conditions (process, voltage, and temperature) unless stated otherwise.(70°C)

Table 13. Current consumption

Device State	Average current consumption				Unit
	AVDD		IOVDD		
	Typ.	Max.	Typ.	Max.	
ULP idle	0.5	2	0	0.5	µA
LP idle	45	300	0.1	1	µA
HP idle (I^2C)(1)	1.3	1.6	2.8	35	mA
HP idle (SPI)(1)	6.4		14.3		mA
Active Ranging(2)	45	50	50	80	mA

1. *HP idle is greater when using the SPI interface as the PLL is maintained to support the SPI clocking*
2. *Active ranging is when the device is actively ranging. The current consumption is not affected by 4x4 or 8x8 zone configuration*

IOVDD peak current will be the average value +10mA.
AVDD peak current will be the average current +10mA.

Table 14. Typical power consumption

Parameter	2V8/1V8	2V8/2V8	3V3/3V3	Unit
4x4 mode - 1Hz frame rate with 5ms integration time, autonomous	3.1	3.9	4.8	mW
4x4 mode - 5Hz frame rate with 5ms integration time	17.8	22.8	29.5	
4x4 mode - 10Hz frame rate with 45ms integration time	202	249	303.5	
8x8 mode - 1Hz frame rate with 5ms integration time -interrupt mode	13.77	17.64	17.54	

5.5 Digital input and output

The following tables summarize the digital I/O electrical characteristics.

Table 15. SPI, GPIO1 and GPIO2

Symbol	Parameter	IOVDD configuration	Min.	Max.	Unit
V_{IL}	Low level input voltage	1.8 V	-0.3	0.35* IOVDD	V
		2.8V - 3.3V			
V_{IH}	High level input voltage	1.8 V	0.65*IOVDD	2.28	
		2.8V - 3.3V		3.6	

Symbol	Parameter	IOVDD configuration	Min.	Max.	Unit
V_{OL}	Low level output voltage (I_{OUT} = 4 mA)	1.8 V	—	0.4	V
		2.8 V - 3.3V			
V_{OH}	High level output voltage (I_{OUT} = 4 mA)	1.8 V	1.22	—	
		2.8 V - 3.3 V	2.1		

Table 16. I^2C interface (SDA/SCL)

Symbol	Parameter	IOVDD configuration	Min.	Max.	Unit
V_{IL}	Low level input voltage	1.8 V	-0.3	0.54	V
		2.8 V - 3.3 V		0.3*IOVDD	
V_{IH}	High level input voltage	1.8 V	1.13	2.28	
		2.8 V - 3.3 V		3.6	
V_{OL}	Low level output voltage (I_{out} = 4 mA)	1.8 V	—	0.4	
		2.8 V- 3.3 V			
$I_{IL/IH}$	Leakage from IOVDD supply		—	2.5	µA
	Leakage from IOVDD pad		—	1	

Note: I^2C pads use 1V8 switching thresholds for all IOVDD supplies

Note: A maximum load of 12mA is assumed in the above table

5.6 Charge pump disable mode

The module uses an internal charge pump to generate a 3V6 voltage from AVDD which is the level required to enable the VCSEL.

However if a user has access to a 3V3 supply that can be guaranteed not to drop below 3V0, then the charge pump may be disabled via the configuration loaded before ranging starts.

Disabling the charge pump may be beneficial in some designs as it will reduce the typical current consumption on AVDD by upto 20mA.

Note: With the VCSEL power supply lowered from 3V6 to 3V0 there may be a small performance drop in ranging upto 6%

Table 17. Recommended limits on AVDD for use when the charge pump is enabled or disabled

charge pump	Min.	Typical	Max.
enabled (default) - VCSEL supply is 3V6	2.5 V	2.8 V	3.3 V
disabled - VCSEL supply is AVDD	3.0 V	3.3 V	3.6 V

6 Ranging performance

6.1 Continuous mode ranging

6.1.1 Measurement conditions

The following criteria and test conditions apply to all the characterisation results detailed in this section unless specified otherwise:

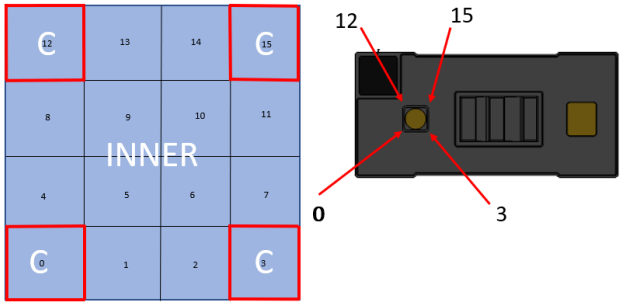
- The specified target fills 100% of the field of view of the device (in all zones).
- Targets used are Munsell N4.75 (17% - measured as 13% IR reflectance at 940nm) and Munsell N9.5 (88% visible and IR reflectance).
- AVDD is 2.8 V, IOVDD is 1.8 V.
- Nominal ambient temperature is 23 ^{o}C.
- Maximum range capability is based on a 100% detection rate.
- Range accuracy figures are based on 2.7 sigma ie 99.3% of measurements are within the specified accuracy.
- Tests are performed in the dark and 2W/m^2 target illumination (940nm). 2 W/m^2 target irradiance at 940nm is equivalent to 5kLux daylight.
- All tests are performed without coverglass.
- Calibration is performed on each device before each measurement.
- The device is controlled through the API.

6.1.2 Zone mapping

6.1.2.1 Zone mapping 4x4

The figure below shows the zone definition in 4x4 mode. There are 16 zones in total which increment along a row first before starting a new row. The physical view is from the device top into the lens. The numbers of each zone, as indicated in the figure below, correspond to the ZoneIDs returned by the sensor.

Figure 24. Zone mapping in 4x4 mode

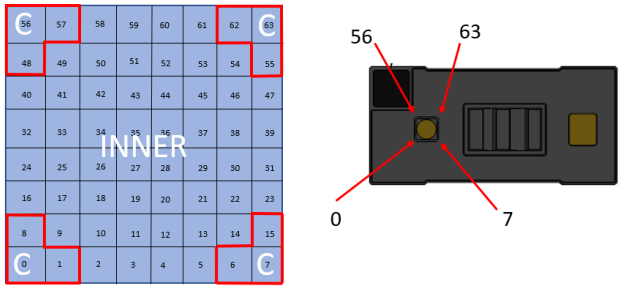


C = Corner zones
INNER = all zones not identified as the corner

6.1.2.2 Zone mapping 8x8

The figure below shows the zone definition in 8x8 mode. There are 64 zones in total which increment along a row first before starting a new row. The physical view is from the device top into the lens. The numbers of each zone, as indicated in the figure below, correspond to the ZoneIDs returned by the sensor to the host.

Figure 25. **Zone mapping in 8x8 mode**

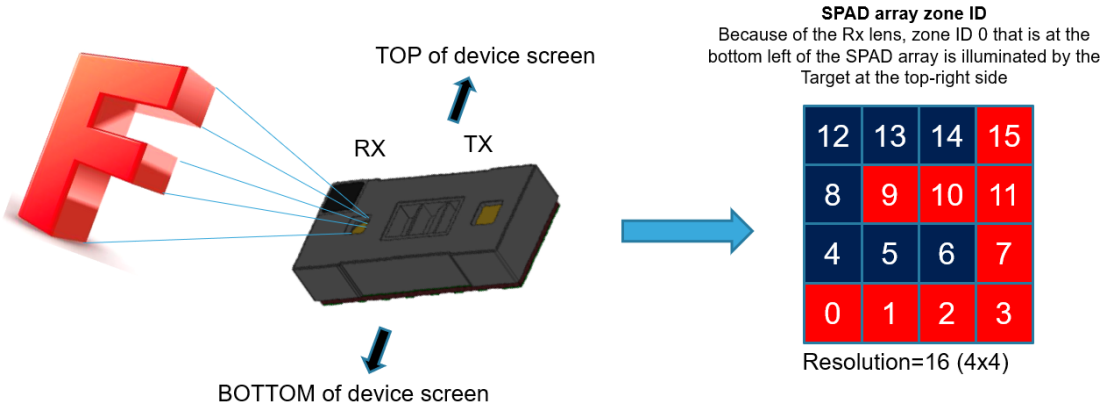


C = Corner zones
INNER = all zones not identified as the corner

6.1.2.3 *Effective zone orientation*

The VL53L5 module includes a lens over the RX aperture which flips (horizontally and vertically) the captured image of the target. As a consequence, the zone identified as zone 0 in the bottom left of the SPAD array is illuminated by a target located at the top right hand side of the scene.

Figure 26. **Effective orientation**



6.1.3 Maximum ranging distance 4x4

The table below shows the maximum ranging capability of the VL53L5 under different conditions. Refer to section 6.1 for the general test conditions.

Table 18. **Max ranging capabilities when ranging continuously at 30Hz**

Target reflectance level. Full FoV (reflectance %)	Zone	Dark	Light (5 klux)
White target (88%)	Inner	Typical: 4000 mm Minimum: 4000 mm	Typical: 950 mm Minimum: 850 mm
	Corner	Typical: 4000 mm Minimum: 4000 mm	Typical: 900 mm Minimum: 800 mm
Grey target (17%)(1)	Inner	Typical: 2400 mm Minimum: 1900 mm	Typical: 800 mm Minimum: 700 mm
	Corner	Typical: 2200 mm Minimum: 1800 mm	Typical: 750 mm Minimum: 650 mm

1. *measured 13% in IR at 940nm*

6.1.4 Maximum ranging distance 8x8

The table below shows the maximum ranging capability of the VL53L5 under different conditions. Refer to section 6.1 for the general test conditions.

Table 19. Max ranging capabilities when ranging continuously at 15Hz

Target reflectance level. Full FoV (reflectance %)	Zone	Dark (0 klux)	Light (5 klux)
White target (88%)	Inner	Typical: 3500 mm Minimum: 2600 mm	Typical: 750 mm Minimum: 650 mm
	Corner	Typical: 3100 mm Minimum: 1700 mm	Typical: 700 mm Minimum: 500 mm
Grey target (17%)(1)	Inner:	Typical: 1300 mm Minimum: 900 mm	Typical: 450 mm Minimum: 400 mm
	Corner	Typical: 1100 mm Minimum: 600 mm	Typical: 450 mm Minimum: 250 mm

1. *measured 13% in IR at 940nm*

6.1.5 Range accuracy

The figure below illustrates how range accuracy is defined over distance.

Figure 27. Range accuracy vs distance

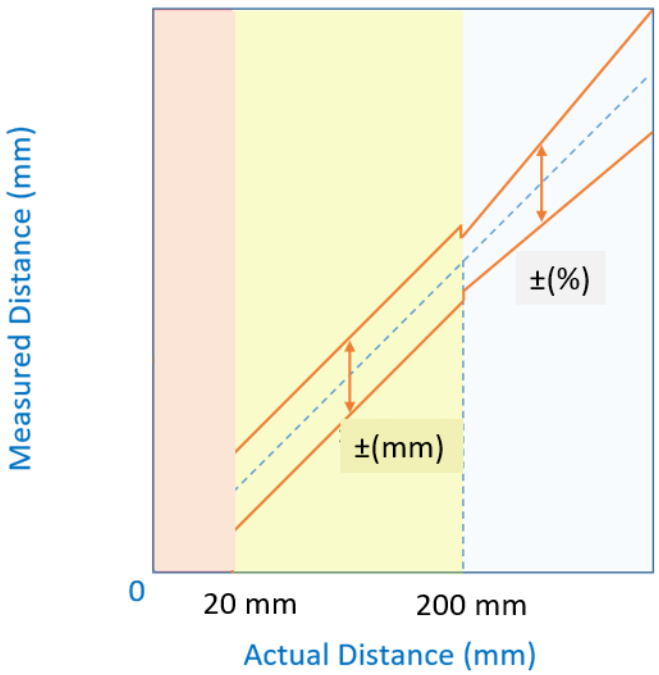


Table 20. Range accuracy

Distance	Mode	Target reflectance	Zones	Dark (0 klux)	Light (5 klux)
20 - 200 mm	8x8 15Hz	Grey target (13%)	All	15 mm	15 mm

Distance	Mode	Target reflectance	Zones	Dark (0 klux)	Light (5 klux)
201 - 4000 mm	4x4 30Hz	White target (88%)	All	4%	7%
		Grey target (13%)		5%	8%
	8x8 15Hz	White target (88%)		5%	8%
		Grey target (13%)		5%	11%

6.2 Autonomous mode ranging

6.2.1 Measurement conditions

The following criteria and test conditions apply to all the characterisation results detailed in this section unless specified otherwise:

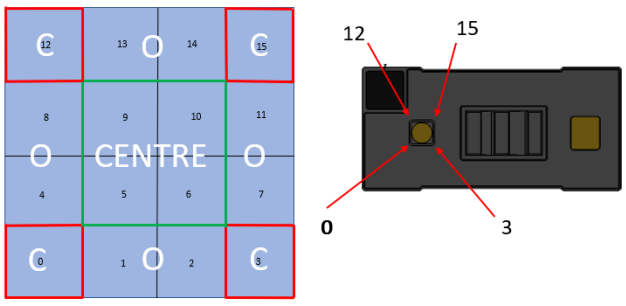
- The specified target fills 100% of the field of view of the device (in all zones).
- Targets used are 56% reflectance.
- AVDD is 2.8 V, IOVDD is 1.8 V.
- Nominal ambient temperature is 23 ^{o}C.
- Maximum range capability is based on a 99% detection rate.
- Range accuracy figures are based on 2.7 sigma ie 99.3% of measurements are within the specified accuracy.
- Tests are performed at 3 ambient light levels, 0 kcps/spad, 10 kcps/spad (80 lux) and 60 kcps (500 lux).
- Measurements are from 20cm to maximum detected range with 10cm steps
- All tests are performed without coverglass.
- Calibration relies on NVM data for RefSpad and Offset, a correction of 50kcps/spad peak is applied for Xtalk.
- The device is controlled through the API.

6.2.2 Zone mapping

6.2.2.1 *Zone mapping 4x4*

The figure below shows the zone definitions in 4x4 mode. There are 16 zones in total which increment along a row first before starting a new row. The physical view is from the device top into the lens. The numbers of each zone, as indicated in the figure below, correspond to the ZoneIDs returned by the sensor to the host.

Figure 28. Zone mapping in 4x4 mode

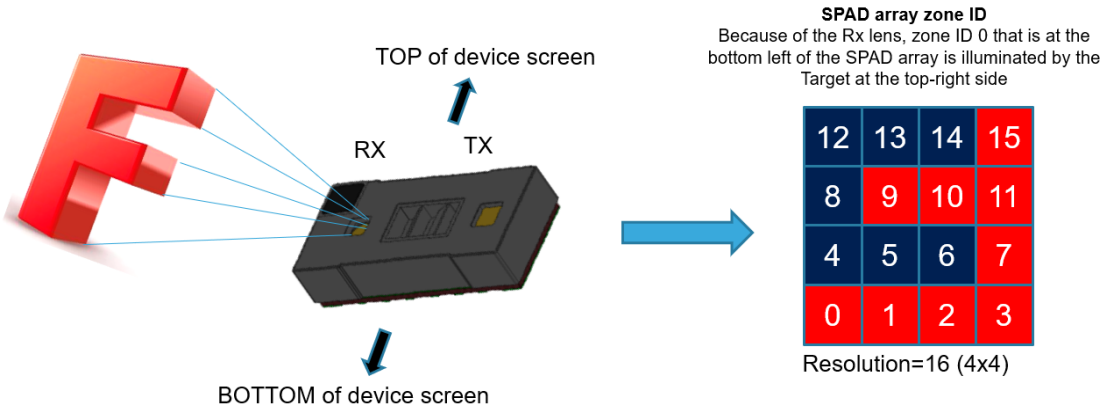


C = Corner zones
CENTRE = 4 centre zones
O = Other

6.2.2.2 *Effective zone orientation*

The VL53L5 module includes a lens over the RX aperture which flips (horizontally and vertically) the captured image of the target. As a consequence, the zone identified as zone 0 in the bottom left of the SPAD array is illuminated by a target located at the top right hand side of the scene.

Figure 29. **Effective orientation**



6.2.3 Maximum ranging distance 4x4

The table below shows the maximum ranging capability of the module under different timed mode conditions. Refer to section 6.1 for the general test conditions.

Table 21. **Max ranging capabilities with a 56% reflectance target**

Frame rate	Integration time	Zone	0 kcps/spad (0 lux)	10 kcps/spad (80 lux)	60 kcps/spad (500 lux)
5 Hz (200 ms)	5 ms	Centre	Typical: 3000 mm Minimum: 2800 mm	Typical: 2300 mm Minimum: 2000 mm	Typical: 1500 mm Minimum: 1300 mm
		Other	Typical: 2300 mm Minimum: 2000 mm	Typical: 2000 mm Minimum: 1700 mm	Typical: 1400 mm Minimum: 1300 mm
		Corner	Typical: 2000 mm Minimum: 1700 mm	Typical: 1800 mm Minimum: 1600 mm	Typical: 1300 mm Minimum: 1200 mm
10 Hz (100 ms)	45 ms	Centre	Typical: 3000 mm Minimum: 3000 mm	Typical: 3000 mm Minimum: 3000 mm	Typical: 2700 mm Minimum: 2400 mm
		Other	Typical: 3000 mm Minimum: 2300 mm	Typical: 2800 mm Minimum: 2200 mm	Typical: 2200 mm Minimum: 2000 mm
		Corner	Typical: 2500 mm Minimum: 2000 mm	Typical: 2400 mm Minimum: 1900 mm	Typical: 2000 mm Minimum: 1800 mm

6.2.4 Range accuracy

Ranging accuracy shall be within ±5% of reported range above 30 cm.

6.3 Range offset drift over temperature

Any increase in silicon temperature either from self-heating or a change in ambient temperature results in a range offset drift which may be minimised by performing periodic auto-calibration, resulting in typical drift of 0.05 mm/DegC.

Any change in silicon temperature either from self-heating or a change in ambient temperature results in a range offset drift of typically 0.5 mm/DegC. This range drift can be minimized by performing an auto-calibration periodically.

7 Outline drawings

The figures below gives details of the VL53L5 module.

Figure 30. Outline drawing (page 1/4)

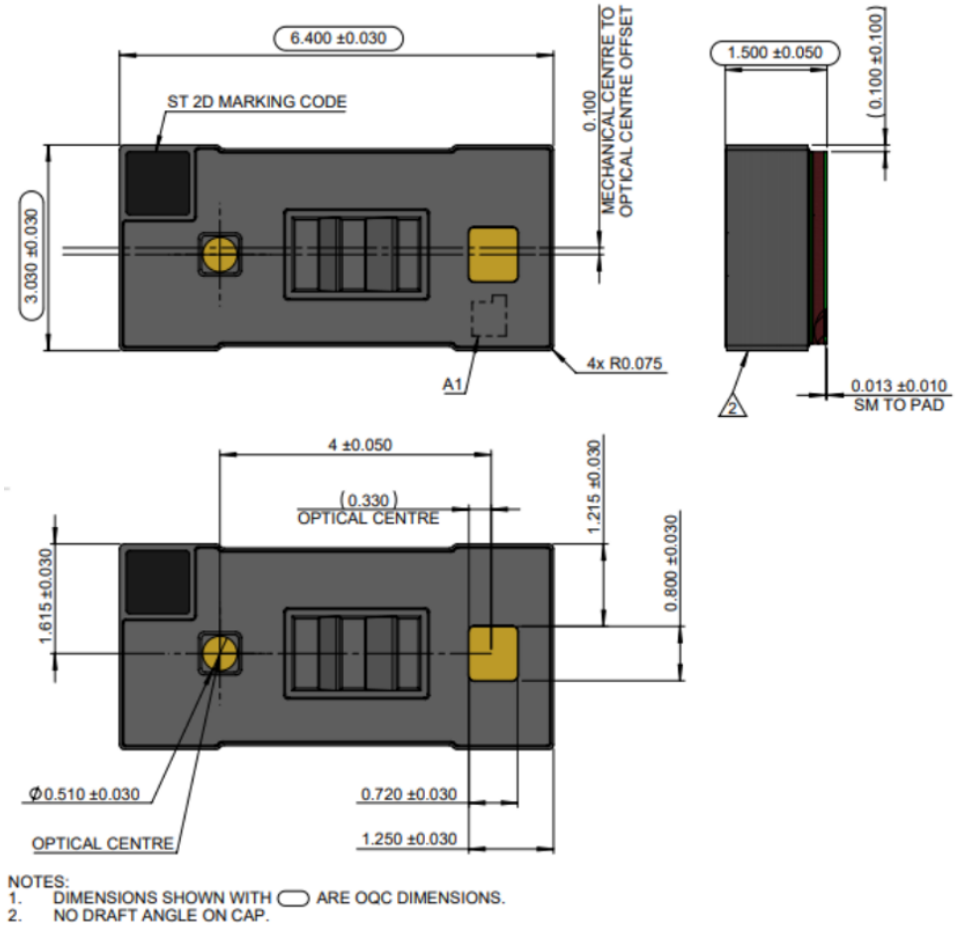
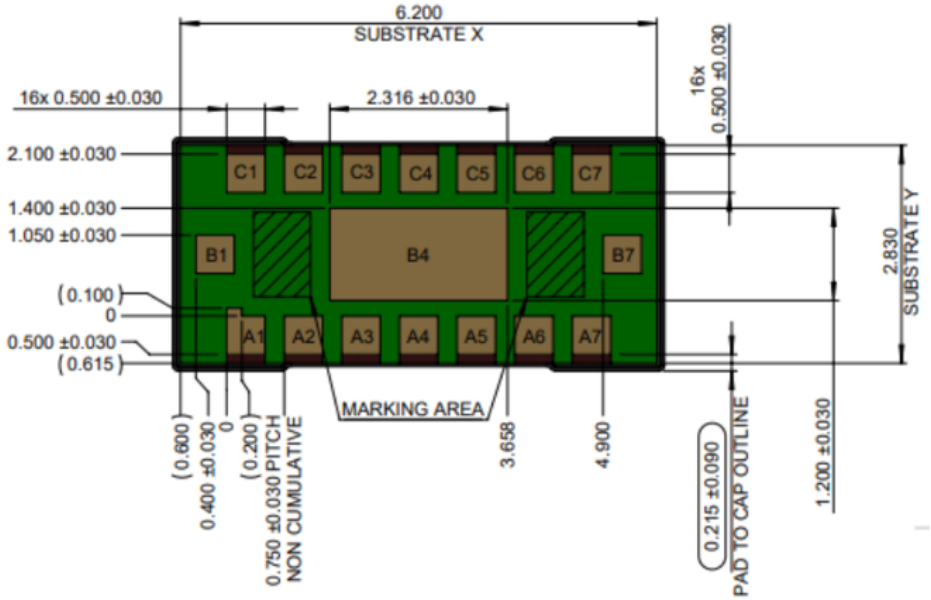


Figure 31. **Outline drawing (page 2/4)**



CONNECTION TABLE

PAD No.	FUNCTION
A1	SPI_12C_N
A2	NCS
A3	GPIO1
A4	IOVDD
A5	LPn
A6	GND
A7	GND
B1	AVDD
B4	THERMAL PAD
B7	AVDD
C1	GND
C2	GPIO2
C3	SDA / MOSI
C4	SCL / MCLK
C5	MISO
C6	GND
C7	GND

Figure 32. **Outline drawing (page(3/4)**

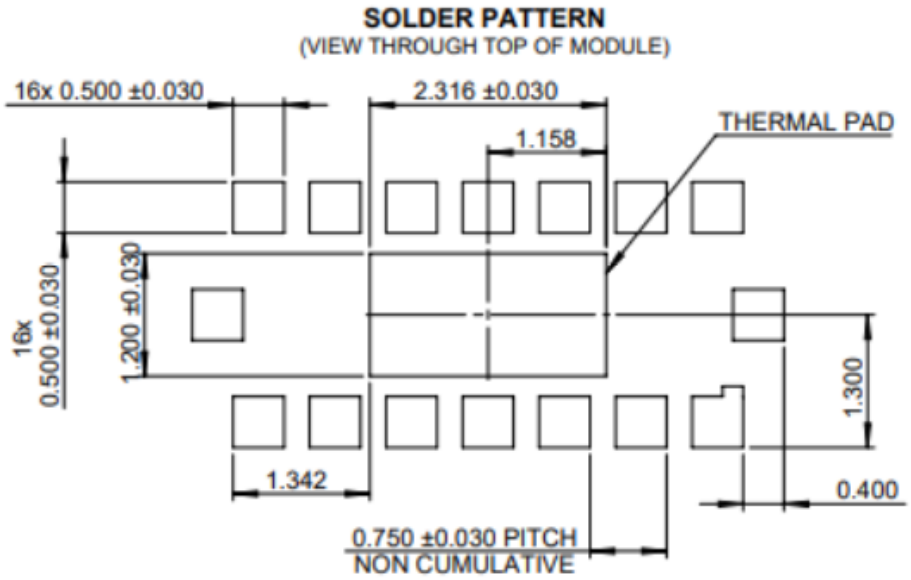
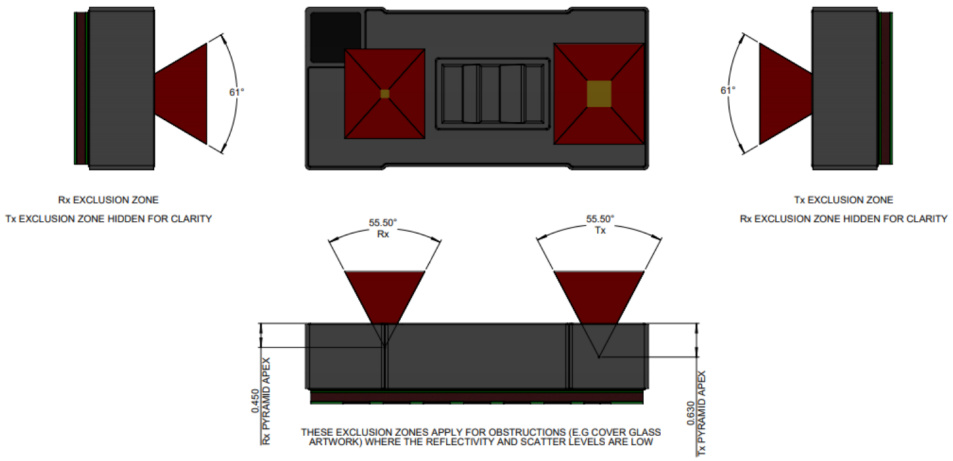


Figure 33. **Outline drawing (page 4/4)**



8 Laser safety considerations

The VL53L5 contains a laser emitter and corresponding drive circuitry. The laser output is designed to remain within Class 1 laser safety limits under all reasonably foreseeable conditions including single faults in compliance with IEC 60825-1:2007 and IEC 60825-1:2014.

The laser output power must not be increased by any means and no optics should be used with the intention of focusing the laser beam.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Figure 34. Class 1 laser label

Figure 35. Laser notice 50: applies to IEC 60825-1:2007

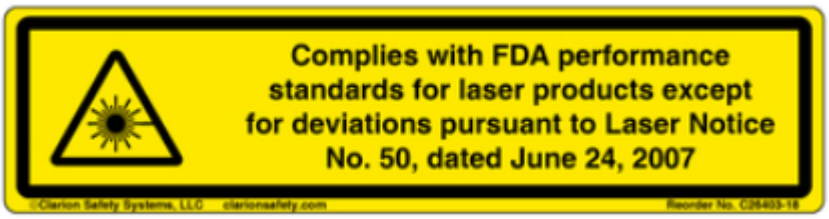
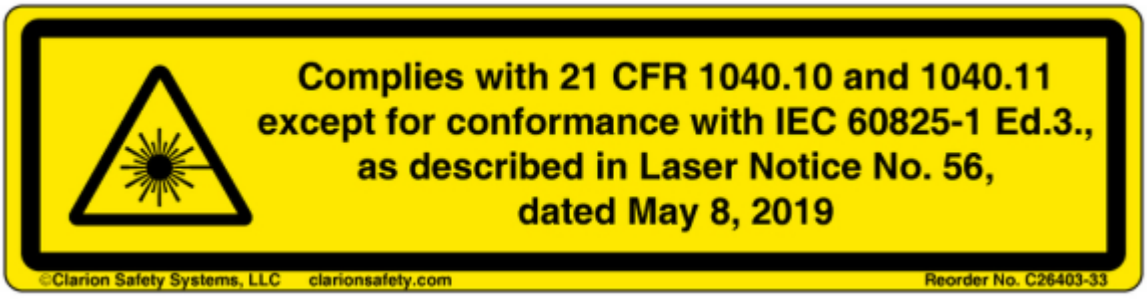


Figure 36. Laser notice 56: applies to IEC 60825-1:2014

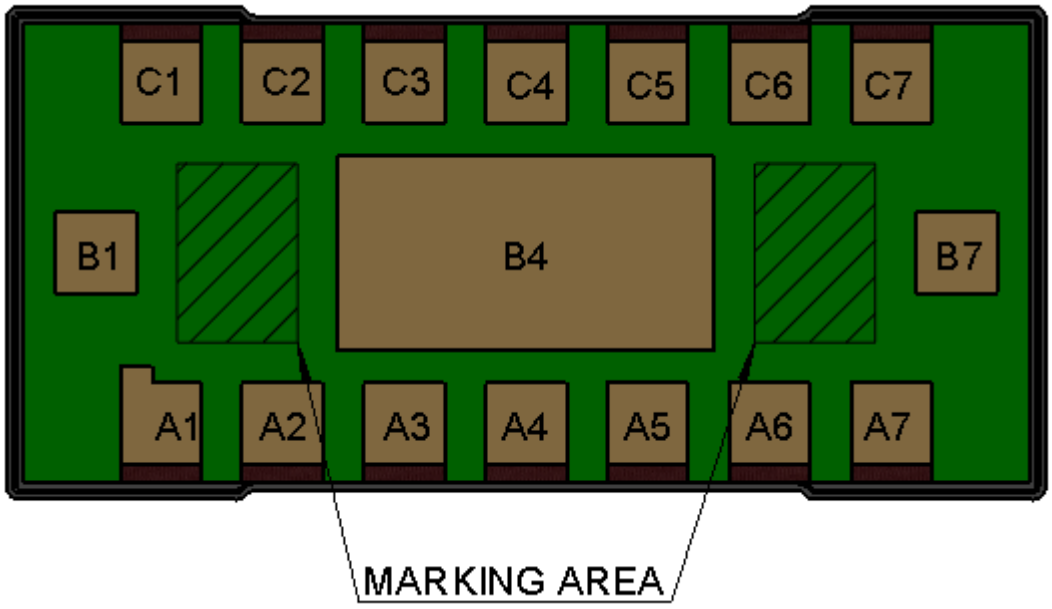


9 Packaging and labelling

9.1 Product marking

See the figure below for the product marking area.
The marking shall be L5C-

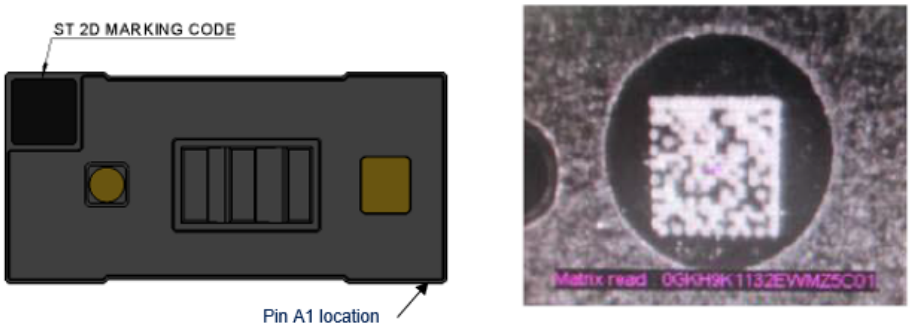
Figure 37. Product marking area



A 2D product marking code is applied on the corner of the module cap as shown in the figure below.

Note: The 2D marking code aligns with pin C7 of the module and is not an indicator of pin 1.

Figure 38. 2D product marking code



9.2 Inner box labelling

The labeling follows the ST standard packing acceptance specification.

The following information is on the inner box label:

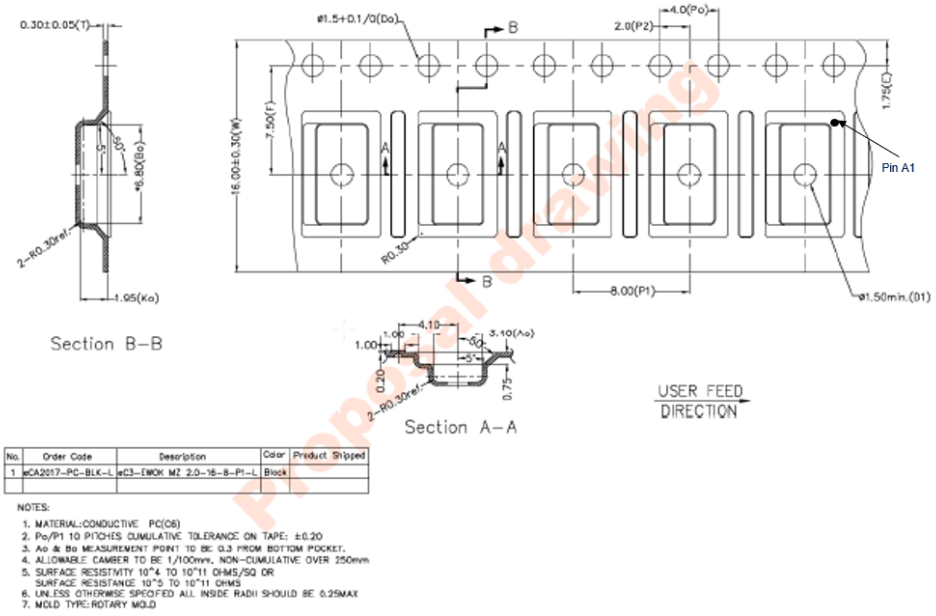
- Assembly site
- Sales type
- Quantity
- Trace code
- Marking
- Bulk ID number

9.3 Packing

The modules are shipped in a tape and reel format (see Section 10 Ordering information). At customer/ subcontractor level, it is recommended to mount the VL53L5 in a clean environment to ensure no contamination of the module laser cavity.

9.4 Tape outline drawing

Figure 39. VL53L5 Tape outline and reel packaging drawing



No.	Order Code	Description	Color	Product Shipped
1	eCA2017-PC-BLK-L	eC3-EMOK MZ 2.0-16-8-Pt-L	Black	

NOTES:
1. MATERIAL:CONDUCTIVE PC(C6)
2. Po/P1 10 PITCHES CUMULATIVE TOLERANCE ON TAPE: ±0.20
3. Ao & Bo MEASUREMENT POINT TO BE 0.3 FROM BOTTOM POCKET.
4. ALLOWABLE CAMBER TO BE 1/100mm, NON-CUMULATIVE OVER 250mm
5. SURFACE RESISTIVITY 10^4 TO 10^11 OHMS/SQ OR
SURFACE RESISTANCE 10^5 TO 10^11 OHMS
6. UNLESS OTHERWISE SPECIFIED ALL INSIDE RADII SHOULD BE 0.25MAX
7. MOLD TYPE:ROTARY MOLD

9.5 Pb-free solder reflow process

The table and figure below show the recommended and maximum values for the solder profile.

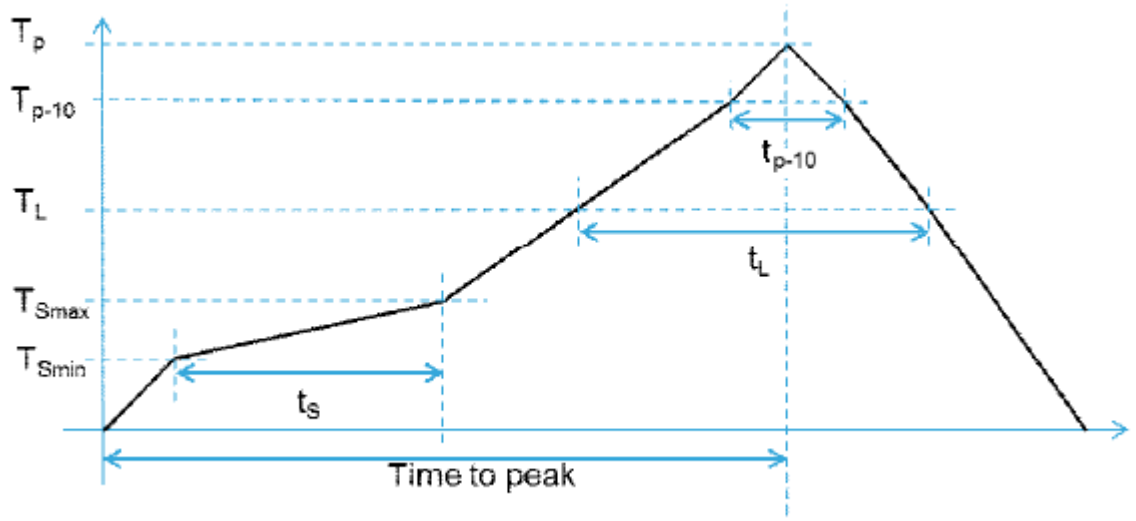
Customers have to tune the reflow profile depending on the PCB, solder paste and material used. We expect customers to follow the “recommended” reflow profile, which is specifically tuned for the VL53L5 package.

For any reason, if a customer must perform a reflow profile which is different from the “recommended” one (especially peak >240 °C), the new profile must be qualified by the customer at their own risk. In any case, the profile has to be within the “maximum” profile limit described in the table below.

Table 22. Recommended solder profile

Parameters	Recommended	Maximum	Units
Minimum temperature (T_S min)	130	150	°C
Maximum temperature (T_S max)	200	200	°C
Time t_s (T_S min to T_S max)	90-110	60-120	s
Temperature (T_L)	217	217	°C
Time (t_L)	55-65	55-65	s
Ramp up	2	3	°C/s
Temperature (T_{p-10})	—	235	°C
Time (t_{p-10})	—	10	s
Ramp up	—	3	°C/s
Peak temperature (T_p)	240	260	°C
Time to peak	300	300	s
Ramp down (peak to T_L)	-4	-6	°C/s

Figure 40. Solder profile



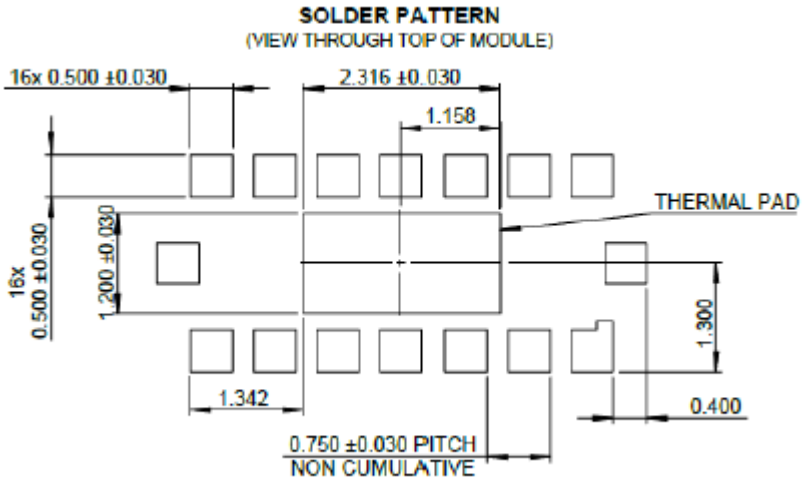
Note: The component should be limited to a maximum of three passes through this solder profile.

Note: As the VL53L5 package is not sealed, only a dry reflow process should be used (such as convection re-flow). Vapor phase reflow is not suitable for this type of optical component.

Note: The VL53L5 is an optical component and as such, it should be treated carefully. This would typically include using a 'no-wash' assembly process.

9.6 Recommended solder pad dimensions

Figure 41. Recommended solder pattern



9.7 Handling and storage precautions

9.7.1 Shock precautions

Sensor modules house numerous internal components that are susceptible to shock damage. If a unit is subject to excessive shock, is dropped on the floor, or a tray/reel of units is dropped on the floor, it must be rejected, even if no apparent damage is visible.

9.7.2 Part handling

Handling must be done with non-marring ESD safe carbon, plastic, or teflon tweezers. Ranging modules are susceptible to damage or contamination. The customer is advised to use a clean assembly process until a protective cover glass is mounted.

9.7.3 Compression force

A maximum compressive load of 25 N should be applied on the module.

9.7.4 Moisture sensitivity level

Moisture sensitivity is level 3 (MSL) as described in IPC/JEDEC JSTD-020-C.

Note: If devices are stored out of the packaging for greater than 168hrs, the devices should be baked before use. The optimum bake recommended is at +90°C for a minimum of 6 hours.

9.8 Storage temperature conditions

Table 23. Recommended storage conditions

Parameter	Min.	Typ.	Max.	Unit
Temperature (storage)	-40	23	90	°C

10 Ordering information

VL53L5 is currently available in the formats below. More detailed information is available on request.

Table 24. Order codes

Order codes	Package	Packing	Minimum order quantity
VL53L5CAV0GC/1	Optical LGA16 without liner	Tape and reel	3600 pcs

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

12 Acronyms and abbreviations

Table 25. **Acronyms and abbreviations**

Acronym/abbreviation	Definition
AF	autofocus
API	application programming interface
AR/VR	augmented reality/virtual reality
DOE	diffractive optical element
ESD	electrostatic discharge
FoV	field of view
GPIO	general purpose input output
HP	high power
I^2C	inter-integrated circuit (serial bus)
LGA	land grid array
LP	low power
NVM	non-volatile memory
PCB	printed circuit board
PDAF	phase detection autofocus
PLL	phase-locked loop
PVT	Process Voltage and Temperature
POR	power on reset
RAM	random-access memory
ROI	region of interest
SPAD	single photon avalanche diode
SPI	serial peripheral interface
SW	software
ToF	Time-of-Flight
UI	user interface
ULP	ultra low power
UM	user manual
VCSEL	vertical cavity surface emitting laser

Revision history

Table 26. **Document revision history**

Date	Version	Changes
02-May-2019	1	Initial release
04-Apr-2020	2	Remove reflectance from FIDA application Add 3.3V to features, table 1 and table 2 for IOVDD/AVDD supplies Add new FoV section Updated figures 3-6 Updated power state diagram Update power up slew details Update current consumption added autonomous power figures update I2C switching - 1.8V levels regardless of IOVDD added typical power consumption table Adding section 6 on performance characteristics removed liner drawing removed CB from order info Updated T&R figure to show pin A1 update MSL baking advice 90C/6hrs - storage max 90C from 125
31-Jul-2020	3	Added CP collapse section Added effective zone map sections Updated max temp to 85C updated block diag updated autonomous mode setup updated applications details

Contents